

WHAT IS CLAIMED IS:

1 1. A method for fabricating an integrated circuit
2 comprising the steps of:

3 fabricating a portion of an integrated circuit
4 comprising at least one active circuit area; and

5 fabricating a redistribution metal layer in said
6 integrated circuit during a fabrication process of said
portion of said integrated circuit.

1 2. The method as set forth in Claim 1 further
2 comprising the step of:

3 fabricating portions of said redistribution metal
4 layer that are open to receive a solder bump.

1 3. The method as set forth in Claim 1 further
2 comprising the steps of:

3 fabricating an active circuit area and an associated
4 metal pad on a base substrate;

5 fabricating a vertical plug of a redistribution metal
6 layer;

7 mounting said vertical plug of said redistribution
8 metal layer on said metal pad;

9 electrically connecting said vertical plug of said
10 redistribution metal layer to said metal pad;

11 depositing an undoped silicon oxide layer on said
12 active circuit area and on said metal pad;

13 depositing a phosphosilicate glass layer on said
14 undoped silicon oxide layer;

15 depositing a silicon oxynitride layer over said
16 phosphosilicate glass layer;

17 depositing a flat redistribution metal layer over said
18 silicon oxynitride layer; and

19 electrically connecting said flat redistribution metal
20 layer to said vertical plug of said redistribution metal
21 layer.

1 4. The method as set forth in Claim 3 further
2 comprising the steps of:

3 depositing a polyimide layer over portions of said
4 flat redistribution metal layer and over portions of said
5 silicon oxynitride layer; and

6 etching portions of said polyimide layer to leave
7 portions of said flat redistribution metal layer open to
8 receive a solder bump.

1 5. The method as set forth in Claim 1 further
2 comprising the steps of:

3 fabricating an active circuit area and an associated
4 metal pad on a base substrate;

5 depositing an undoped silicon oxide layer on said
6 active circuit area and on said metal pad;

7 depositing a phosphosilicate glass layer on said
8 undoped silicon oxide layer;

9 depositing a redistribution metal layer over said
10 phosphosilicate glass layer;

11 electrically connecting said redistribution metal
12 layer to said metal pad; and

13 depositing a silicon oxynitride layer over portions of
14 said redistribution metal layer.

1 6. The method as set forth in Claim 5 further
2 comprising the step of:

3 leaving portions of said redistribution metal layer
4 open to receive a solder bump.

1 7. The method as set forth in Claim 5 further
2 comprising the step of:

3 depositing a silicon oxynitride layer over all
4 portions of said redistribution metal layer.

1 8. The method as set forth in Claim 7 further
2 comprising the step of:

3 etching said silicon oxynitride layer to a pattern
4 that leaves portions of said redistribution metal layer
5 uncovered to receive a solder bump.

1 9. The method as set forth in Claim 5 further
2 comprising the steps of:

3 depositing a polyimide layer over portions of said
4 redistribution metal layer and over portions of said
5 silicon oxynitride layer; and

6 etching portions of said polyimide layer to leave
7 portions of said flat redistribution metal layer open to
8 receive a solder bump.

1 10. The method as set forth in Claim 1 further
2 comprising the step of:

3 fabricating said redistribution metal layer using a
4 last metal layer that is used to fabricate an active
5 circuit area of said integrated circuit.

1 11. An integrated circuit comprising:

2 a portion of an integrated circuit comprising at least
3 one active circuit area; and

4 a redistribution metal layer in said integrated
5 circuit fabricated during a fabrication process of said
6 portion of said integrated circuit.

12. The integrated circuit as set forth in Claim 11
wherein portions of said redistribution metal layer in said
integrated circuit are open to receive a solder bump.

13. The integrated circuit as set forth in Claim 11
further comprising:

an active circuit area and an associated metal pad on
4 a base substrate;

5 a vertical plug of a redistribution metal layer
6 mounted on and electrically connected to said metal pad;

7 a layer of undoped silicon oxide layer deposited on
8 said active circuit area and on said metal pad;

9 a phosphosilicate glass layer deposited on said
10 undoped silicon oxide layer;

11 a silicon oxynitride layer deposited on said
12 phosphosilicate glass layer; and

13 a flat redistribution metal layer deposited over said
14 silicon oxynitride layer;

15 wherein said flat redistribution metal layer is
16 electrically connected to said vertical plug of said
17 redistribution metal layer.

14. The integrated circuit as set forth in Claim 13
further comprising:

a polyimide layer deposited over portions of said flat
redistribution metal layer and over portions of said
silicon oxynitride layer;

wherein said polyimide layer is etched to leave
portions of said flat redistribution metal layer open to
receive a solder bump.

15. The integrated circuit as set forth in Claim 11
further comprising:

an active circuit area and an associated metal pad on
a base substrate;

an undoped silicon oxide layer deposited on said
active circuit area and on said metal pad;

7 a phosphosilicate glass layer deposited on said
8 undoped silicon oxide layer;

9 a redistribution metal layer deposited over said
10 phosphosilicate glass layer, wherein said redistribution
11 metal layer is electrically connected to said metal pad;
12 and

13 a silicon oxynitride layer deposited over portions of
14 said redistribution metal layer.

16. The integrated circuit as set forth in Claim 15
wherein portions of said redistribution metal layer are
open to receive a solder bump.

17. The integrated circuit as set forth in Claim 15
further comprising:

3 a silicon oxynitride layer deposited over said
4 redistribution metal layer etched to a pattern that leaves
5 portions of said redistribution metal layer uncovered to
6 receive a solder bump.

1 18. The integrated circuit as set forth in Claim 15
2 further comprising:

3 a polyimide layer deposited over portions of said
4 redistribution metal layer and over portions of said
5 silicon oxynitride layer;

6 wherein portions of said redistribution metal layer
7 are open to receive a solder bump.

1 19. The integrated circuit as set forth in Claim 11
2 further comprising:

3 a redistribution metal layer fabricated using a last
4 metal layer that is used to fabricate an active circuit
5 area of said integrated circuit.

1 20. The integrated circuit as set forth in Claim 12
2 further comprising:

3 a solder bump attached to said portions of said
4 redistribution metal layer of said integrated circuit that
5 are open to receive a solder bump.

1 21. The integrated circuit as set forth in Claim 14
2 further comprising:

3 a solder bump attached to said portions of said flat
4 redistribution metal layer of said integrated circuit that
5 are open to receive a solder bump.

1 22. The integrated circuit as set forth in Claim 16
2 further comprising:

3 a solder bump attached to said portions of said flat
4 redistribution metal layer of said integrated circuit that
5 are open to receive a solder bump.

1 23. A method for fabricating an integrated circuit
2 comprising the steps of:

3 fabricating a first portion of an active circuit area
4 and an associated metal pad on a base substrate, said first
5 portion of said active circuit area comprising a next to
6 last metal layer;

7 depositing a passivation layer on said first portion
8 of said active circuit area and on said metal pad;

9 etching at least one via through said passivation
10 layer to said metal pad;

11 etching a metal layer pattern into said passivation
12 layer;

13 depositing a last metal layer onto said metal layer
14 pattern on said passivation layer to form a redistribution
15 metal layer; and

16 depositing said last metal layer onto said first
17 portion of said active circuit area to form a complete
18 active circuit area.

1 24. The method as claimed in Claim 23 further
2 comprising the step of:

3 polishing a surface of said redistribution metal layer
4 to produce a flat surface on said redistribution metal
5 layer.

1 25. The method as claimed in Claim 23 further
2 comprising the step of:

3 depositing said last metal layer into at least one via
4 to electrically connect said metal pad to said
redistribution metal layer.

1 26. An integrated circuit comprising:

2 a first portion of an active circuit area and an
3 associated metal pad on a base substrate, said first
4 portion of said active circuit area comprising a next to
5 last metal layer;

6 a passivation layer deposited on said first portion of
7 said active circuit area and on said metal pad;

8 at least one via etched through said passivation layer
9 to said metal pad;

10 a metal layer pattern etched into said passivation
11 layer; and

12 a redistribution metal layer deposited on said metal
13 layer pattern in said passivation layer, wherein said
14 redistribution metal layer comprises a last metal layer,
15 and wherein a portion of said last metal layer is deposited
16 on said first portion of said active circuit area to form a
17 complete active circuit area.

1 27. The integrated circuit as claimed in Claim 26
2 comprising metal within said at least one via, wherein said
3 metal within said at least one via forms a unitary
4 structure with said redistribution metal layer.

1 28. The integrated circuit as claimed in Claim 27
2 wherein said metal within said at least one via
3 electrically connects said metal pad to said redistribution
4 metal layer.

1 29. The integrated circuit as claimed in Claim 26
2 wherein a surface of said redistribution metal layer
3 deposited on said metal layer pattern in said passivation
4 layer comprises a flat surface open to receive a solder
bump.

2 30. The integrated circuit as claimed in Claim 29
further comprising:

4 a solder bump attached to said flat surface of said
redistribution metal layer open to receive a solder bump.